REMARKS

Applicants are amending independent claim 1. Thus, claims 1-5 currently are pending and are subject to examination in the above-captioned patent application. No new matter is added by the foregoing amendments, and these amendments are fully supported by the specification. Applicants respectfully request that the Examiner reconsider the above-captioned patent application in view of the foregoing amendments and the following remarks.

The Examiner rejected claims 1-5 under 35 U.S.C. § 112, ¶ 2, as allegedly being indefinite for failing to particularly point and out and distinctly claim the subject matter that Applicants regard as the invention. Specifically, the Examiner asserts that the logic circuit and the second switching circuit of claims 1-5 are not supported by the specification, as filed. Applicants have amended independent claim 1 in order to clarify that the reference voltage generation circuit includes a first switching circuit, e.g., transistor Tr13 of Figure 11, and a second switching circuit, e.g., transistor Tr14 of Figure 11. Moreover, Applicants respectfully submit that the logic circuit of claims 1-5 may correspond to the logic circuit depicted in Figures 3 and 4. As such, Applicants respectfully submit that the logic circuit and the second switching circuit, as set for in claims 1-5, is supported by the specification, as filed. Therefore, Applicants respectfully request that the Examiner withdraw the indefiniteness rejection of claims 1-5 at least for this reason.

The Examiner also rejected claim 1 under 35 U.S.C. § 102(e), as allegedly being anticipated by U.S. Patent No. 6,624,673 to Kim. Applicants respectfully disagree, and traverse this rejection, as follows.

Applicants' independent claim 1 claims a reference voltage generation circuit and a second switching circuit for starting the reference voltage generation circuit in response to a start signal.

In contrast to Applicants claimed invention as set forth independent claim 1, Kim describes a circuit that stops supplying power to a low voltage detector 16 if a microcontroller enters into a halt mode. The Examiner asserts that the low voltage detector 16 and a delay 14 correspond to Applicants' claimed reference voltage generation circuit and second switching circuit, respectively. However, Applicants respectfully note that the low voltage detector 16 only detects whether a power supply voltage is less than or equal to a threshold value. The delay 14 merely delays an output signal of a flip-flop 12, and sends a delayed signal to a NMOS transistor. However, the delay does not function to start the low voltage detector, and as such, cannot correspond to Applicants' claimed second switching circuit. Therefore, Applicants respectfully request that the Examiner withdraw the anticipation rejection of independent claim 1 at least for this reason.

CONCLUSION

Applicants respectfully submit that the above-captioned patent application is in condition for allowance, and such action is earnestly solicited. If the Examiner believes that an in-person or telephonic interview with Applicants' representatives would expedite the prosecution of the above-captioned patent application, the Examiner is invited to contact the undersigned attorney of records. Applicants believe that no fees are due as a result of this response to the outstanding Office Action in the above-captioned patent application. Nevertheless, in the event of any variance between the fees determined by Applicants and those determined by the U.S. Patent and Trademark Office, please charge any such variance to the undersigned's Deposit Account No. 01-2300.

Respectfully submitted,

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